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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,157	02/17/2004	Monji G. Jabori	200314182-1	1267

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EXAMINER	
RIAD, AMINE	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,157	JABORI, MONJI G.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *13,27 and 28* is/are withdrawn from consideration.

5)☒ Claim(s) *15-17,19,20 and 24* is/are allowed.

6)☒ Claim(s) *1-12,14,18,21-23,25,26,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-30 have been presented for examination.

Claims 13,27,28 have been cancelled.

Claims 1-12,14,18,21,22,23,25,26,29,30 have been rejected.

Claims 15,16,17,19,20,24 have been allowed.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The language of the claims raise a question as to whether the claims are directed merely to an abstract idea that would not result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101.

In summary, Claims 1-12 recite first **logic**, second **logic**, third **logic**, and fourth **logic**. Additionally, page 6 line 7 of the detailed description discloses, "Logic may also be fully embodied as software" The recited invention is computer software *per se*. A computer program is merely a set of instructions capable of being executed by a computer. The computer program itself is not a statutory process in that it does not include the computer-readable medium needed to realize the functionality of the computer program. Thus, as currently recited, Claims 1-12 are directed to an abstract idea that does not produce a concrete, useful and tangible result.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14,18,21,22,23,25,26,29,30 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrett US Patent 6,018,809.

In regard to claims 23, 29

Garrett discloses a correlating debugger, comprising:

Engaging a hardware analyzer to analyze a piece of computer hardware;

Engaging a software analyzer to analyze a piece of computer software that will service (Examiner considers the data collected from the host computer as a combination of hardware data and software data because host computer 22 is a combination of hardware and software) interrupts for the piece of computer hardware; (Column 3; lines 30-31)

Binding the hardware analyzer and the software analyzer together, in order, based on time occurrence; (Column 6; lines 15-17)

Receiving an event from the hardware analyzer and the software analyzer together, in order, based on time of occurrence. (Column 6; lines 35-39)

In regard to claim 14, and 22

Garrett discloses a method, comprising:

- Establishing a relationship in a debugger between a hardware device and a software component that w ill perform a software operation related to the hardware device; (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 19-21) [Each trace engine clock is synchronized with the other trace engine clocks so that all the data collected is synchronized]
- Configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger; [Examiner considers data collected from the SCSI as software data]
- Configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger; (Figure 2; item 38 of figure 3 within trace engine 28) [Examiner considers data collected from the SCSI as hardware data]
- Detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger; (Column 4;lines 40-44)[Examiner points out the interrupt is used for both the hardware and the software]
- Detecting a second event that signals a beginning of the hardware operation (Column 4;lines 40-44)[Examiner points out the interrupt is used for both the hardware and the software]

- controlling the hardware analyzer to begin delivering the second data set to the debugger; and selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred. (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 21-23)

In regard to claim 18,

Garrett discloses the method of claim 14, where configuring the hardware analyzer includes or more of, identifying one or more types of data available in the hardware device to be reported on by the hardware analyzer, and identifying one or more types of events from the hardware device to be reported on by the hardware analyzer.(Garrett discloses that data collected is commands, status , and message information in the background of the invention. Examiner considers this disclosure as an identification)

In regard to claim 21,

Garrett discloses the method of claim 14, where selectively storing together elements of the first data set and elements of the second data set includes selectively adding an element of the second data set to the first data set. (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 21-23) [Since the system contains many trace engines it is inherent to add second data to the already stored first data]

In regard to claim 25,

Garret discloses the method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a logic connection in a correlating debugger configured to receive data from the hardware analyzer and the software analyzer.(Column 3;lines 19-20)[Synchronizing each trace engine's clock necessities a logic connection]

In regard to claim 26,

Garrett discloses the method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a physical connection at a correlating debugger configured to receive data from the hardware analyzer and the software analyzer. (Column 3; lines 22-23) [All trace engines send data to be stored, and finally read by the debugger CPU here]

In regard to claim 30,

Garrett discloses a first logic configures to receive a hardware related debug data from a hardware analyzer (Figure 2; items 20 and 28 [Examiner considers item 28 as a logic connected to item 20]); a second logic configured to receive a software related debug data from a software analyzer (Figure 2; items 20 and 28 [Examiner considers item 28 as a logic connected to item 20]); means for establishing a relationship between the hardware analyzer and the software analyzer to facilitate correlating data received by the first logic and data received by the second logic into a time-ordered set of data. (Column 6; lines 25-29)

Response to Applicant's Argument

Applicant arguments filed on September 1, 2006 have been fully considered, and are not persuasive in view of claims 14,18, and 23.

In regard to the argument concerning claim 14 and 23 which states "while both hardware data and software data my be collected of SCSI bus, this data is not coming from either a hardware analyzer or a software analyzer. The data is coming from either host computer 22 or storage subsystem 24, neither of which is performing a hardware analyzing or a software analyzing function. For at least this reason, claim 14 is not anticipated" Examiner respectfully disagrees. Examiner refers Applicant to Figure 2 where the Examiner considers item 28 as an analyzer, which delivers data to item 20 considered as a debugger. Consequently, the argument is not valid.

In regard to the second part of the argument which states, "The claimed element of configuring the hardware analyzer and the software analyzer is not present" Examiner respectfully disagrees. The configuration of the software analyzer and hardware analyzer is inherent because both analyzers are already collecting data.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
Amine Riad
Patent Examiner
12/13/2006

AR